REMARKS/ARGUMENTS

The Office Action mailed April 25, 2005, has been received and reviewed. Claims 1 through 26 are currently pending in the application. Claims 6 through 20, 22, 25, and 26 have been withdrawn from consideration as being drawn to non-elected invention(s). Claims 1 through 3, 21, 23, and 24 stand rejected. Claims 4 and 5 have been objected to as being dependent upon rejected base claims, but the indication of allowable subject matter in such claims is noted with appreciation. Claims 4 and 5 were objected to and have been amended to include the limitations of the respective base claim. Independent claims 1, 21, 23 and 24 have been amended. No new matter has been added. Applicants respectfully request reconsideration of the application as amended herein.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,068,628 to Ghoshal

Claims 21, 23, and 24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Ghoshal (U.S. Patent No. 5,068,628). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants submit that the Ghoshal references does not and cannot anticipate under 35 U.S.C. § 102 the presently claimed invention of presently amended independent claims 21, 23, and 24, because the Ghoshal reference does not describe, either expressly or inherently, the identical inventions in as complete detail as are contained in the claims.

The Office Action alleges:

> Regarding claim 24, Ghoshal discloses in Fig. 1-9 a variable oscillator circuit (Fig. 1) on a semiconductor device (it is inherent that the circuit is on a semiconductor device), comprising: a means for producing (16, Fig. 2) a variable frequency-oscillating wherein the frequency is varied based on a delay selection signal; a means for analyzing (18 and 20) the frequency of the variable frequency-oscillation signal and converting the analysis results to an encoded actual frequency signal; a means for comparing (10) the encoded actual frequency signal to an encoded desired frequency input and generating a frequency deviation result;

Regarding claims 21 and 23, as discussed above, Figures 1-9 shows variable oscillator circuit, which would necessarily perform the method recited in the claims. (Office Action, pp. 2-3).

Applicants respectfully disagree that the Ghoshal reference anticipates Applicants' invention as claimed in presently amended independent claims 21, 23 and 24 which read:

21. A method for modifying a frequency of an oscillating signal comprising:
generating a variable frequency-oscillating signal using a ring oscillator having a programmable delay magnitude;
analyzing the variable frequency-oscillating signal to develop an encoded actual frequency signal;
comparing the encoded actual frequency signal to an encoded desired frequency input to generate a frequency deviation result; and
modifying the programmable delay magnitude and thereby the variable frequency-oscillating signal, including:
determining an update rate to the variable frequency-oscillating signal by ***dividing the input divide clock by a predetermined programmable rate***;
generating a sampled frequency deviation result based on sampling the frequency deviation result at the update rate; and
generating the delay selection signal based on the sampled frequency deviation result. (Emphasis added.)

23. A method for modifying a frequency of an oscillating signal comprising:
generating a variable frequency-oscillating signal using a ring oscillator having a programmable delay magnitude;
analyzing the variable frequency-oscillating signal to develop an encoded actual frequency signal;
analyzing a reference input clock to develop an encoded desired frequency signal;
comparing the encoded actual frequency signal to the encoded desired frequency signal to generate a frequency deviation result; and
modifying the programmable delay magnitude and thereby the variable frequency-oscillating signal, including:
determining an update rate to the variable frequency-oscillating signal by ***dividing the input divide clock by a predetermined programmable rate***;
generating a sampled frequency deviation result based on sampling the frequency deviation result at the update rate; and
generating the delay selection signal based on the sampled frequency deviation result. (Emphasis added.)

24. A variable oscillator circuit on a semiconductor device, comprising:
a means for producing a variable frequency-oscillating wherein the frequency is varied

based on a delay selection signal;
a means for analyzing the frequency of the variable frequency-oscillating signal and converting the analysis results to an encoded actual frequency signal;
a means for comparing the encoded actual frequency signal to an encoded desired frequency input and generating a frequency deviation result; and
a means for generating the delay selection signal based on the frequency deviation result, ***the means for generating including a clock divider for determining an update rate to the variable frequency-oscillating signal.*** (Emphasis added.)

The Office Action concedes that "the best prior art of record, Ghoshal, taken alone or in combination of other references, does not teach or fairly suggest a clock divider . . .." (Office Action, p. 4).

Therefore, amended independent claims 21, 23 and 24 are not anticipated by the Ghoshal reference under 35 U.S.C. § 102. Accordingly, such claims are allowable over the cited prior art and Applicants respectfully request that such rejections be withdrawn.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,068,628 to Ghoshal in View of U.S. Patent No. 6,114,917 to Nakajima et al.

Claims 1 through 3 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ghoshal (U.S. Patent No. 5,068,628) in view of Nakajima et al. (U.S. Patent No. 6,114,917). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 1 through 3 are improper because the elements for a prima facie case of obviousness are not met. Specifically, the

rejection fails to meet the criterion that the prior art reference must teach or suggest all the claims limitations.

The Office Action states:

> Regarding claim 1, Ghoshal discloses in Fig. 1-9 a variable oscillator circuit (Fig. 1) on a semiconductor device as discussed above (a ring oscillator (16); a frequency analyzer (18, 20); a frequency comparator (10); a frequency modifier (12, 14)). However, Ghoshal does not explicitly disclose an arrangement of ring oscillator as recited in the claimed, i.e., the base delay stage and the variable delay stage, connect in a ring having an odd number of logical inversions."
>
> As would have been well known in the art, such an arrangement of ring oscillator is a typical arrangement that the ring oscillator can be enable or disable based on the base delay stage, for example, Nakajima et al. shows in Fig. 6 a base delay stage, a NAND gate 14 and also shows an odd number logical inversion. (Office Action, p. 3).

In contrast, Applicants amended independent claim 1 recites:

> 1. A variable oscillator circuit on a semiconductor device, comprising:
> a ring oscillator for producing a variable frequency-oscillating signal including:
> a base delay stage; and
> a variable delay stage having a delay selection signal that selects a programmable delay magnitude, wherein
> the base delay stage and the variable delay stage connect in a ring having an odd number of logical inversions;
> a frequency analyzer for converting the variable frequency-oscillating signal to an encoded actual frequency signal;
> a frequency comparator wherein the encoded actual frequency signal is compared to an encoded desired frequency input to generate a frequency deviation result; and
> a frequency modifier for generating the delay selection signal based on the frequency deviation result, the frequency modifier ***including a clock divider for determining an update rate to the variable frequency-oscillating signal.*** (Emphasis added.)

The Office Action concedes that "the best prior art of record, Ghoshal, taken alone or in combination of other references, does not teach or fairly suggest a clock divider . . .." (Office Action, p. 4).

Regarding claim 1 and claims 2 and 3 depending therefrom, Applicants submit that the Ghoshal reference and the Nakajima reference, either individually or in any proper combination, do not teach or suggest Applicants' invention as claimed. Accordingly, Applicants respectfully request the rejection of amended independent claim 1 and claims 2 and 3 depending therefrom be withdrawn.

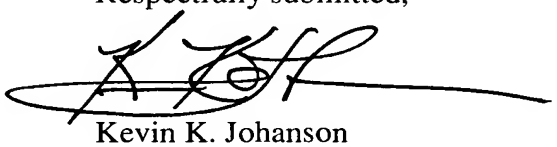
Objections to Claims 4 and 5/Allowable Subject Matter

Claims 4 and 5 stand objected to as being dependent upon rejected base claims, but are indicated to contain allowable subject matter and would be allowable if placed in appropriate independent form. Accordingly, Applicants have amended claims 4 and 5 to include the respective limitations of the corresponding base claim. Applicants respectfully request the objections to claims 4 and 5 be withdrawn.

CONCLUSION

Claims 1-5, 21, 23 and 24 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



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